

WHAT IS CLAIMED IS:

1. An input and output driver comprising:

an input buffer for supplying an input data from a DQ pad to a memory cell array in a writing mode;

5 an output driver for supplying an output data from the memory cell array to the DQ pad in a reading mode; and

 a DQ switch for electrically isolating the output driver from the DQ pad in the writing mode.

10 2. An input and output driver according to claim 1, wherein the DQ switch comprises an NMOS transistor or a PMOS transistor.

 3. An input and output driver according to claim 1, wherein the DQ switch comprises an LVT NMOS transistor or an LVT PMOS transistor.

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 4. An input and output driver according to claim 1, wherein the DQ switch comprises at least two LVT NMOS transistors or at least two LVT PMOS transistors connected in parallel.

20 5. An input and output driver according to claim 1, wherein the DQ switch is a transfer gate.

6. An input and output driver according to claim 5, wherein the transfer gate comprises an LVT NMOS transistor and an LVT PMOS transistor connected in parallel.

5 7. An input and output driver according to claim 6, wherein the LVT NMOS transistor is operated by a pumping voltage or a power source voltage.

8. An input and output driver according to claim 6, wherein the LVT PMOS transistor is operated by a negative pumping voltage or a ground
10 voltage.

9. An input and output driver according to claim 1, wherein the DQ switch is operated by a pumping voltage higher than a power source voltage.

15 10. An input and output driver according to claim 1, wherein a total capacitance of the DQ switch is smaller than that of the output driver.

11. An input and output driver according to claim 1, further comprising an ODT circuit connected between a power source voltage and a
20 node to which the DQ switch and the DQ pad are connected.

12. An input and output driver according to claim 1, further comprising an ESD circuit and a CDM circuit connected between the input buffer and the DQ pad.

13. An input and output driver according to claim 1, wherein the DQ switch is connected between the output driver and the DQ pad.